This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of manufacturing an integrated circuit having a T-shaped gate conductor, the method comprising:

providing a gate dielectric layer above a top surface of a substrate;

providing a silicon and nitrogen containing layer above the gate dielectric layer;

providing an oxide layer above the silicon and nitrogen containing layer;

selectively etching the oxide layer to form a first trench in the oxide layer;

selectively etching the silicon and nitrogen containing layer to form a second trench in the silicon and nitrogen containing layer, the second trench being narrower than the first trench and being disposed below the first trench; and

providing a gate conductor material in the first trench and the second trench to form the T-shaped gate conductor.

2. (Original) The method of claim 1, further comprising removing the oxide layer.

3. (Original) The method of claim 2, further comprising:

removing portions of the silicon and nitrogen containing layer, whereby a pair of spacers remain underneath the gate conductor material in the first trench.

4. (Original) The method of claim 3, wherein the gate conductor material is removed by a polishing process.

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5. (Original) The method of claim 3, wherein the silicon and nitrogen containing layer includes silicon rich nitride.

6. (Currently Amended) The method of claim 1, wherein the selective etching the silicon and nitrogen containing layer includes a selective etching and RELACS process.

7. (Original) The method of claim 1, wherein the silicon and nitrogen containing layer includes SiON or silicon rich nitride.

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8. (Original) The method of claim 7, wherein the silicon and nitrogen containing layer is a silicon rich nitride layer.

9. (Original) The method of claim 1, wherein a width of the first trench is at least 250 Å and less than 1600 Å.

10. (Original) The method of claim 9, wherein the width of the second trench is at least 400 Å and less than 2100 Å.

11. (Currently Amended) A method of manufacturing an ultra-large scale integrated circuit including a transistor with a T-shaped gate conductor, the method includes steps of:

providing a first layer above a substrate, the first containing silicon and nitrogen;

providing an oxide layer over the first layer;

~~forming~~ selectively etching a first trench in the oxide layer by etching;

~~forming~~ selectively etching a second trench by etching in the first layer, the second trench having a smaller width than the first trench; and

providing a gate conductor material in the first trench and in the second trench to form the T-shaped gate conductor.

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12. (Original) The method of claim 11, further comprising removing the oxide layer.

13. (Original) The method of claim 12, further comprising removing portions of the first layer to leave spacers underneath the gate conductor material in the first trench, the removal process utilizing the gate conductor material as a mask.

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14. (Original) The method of claim 13, wherein the first layer is silicon rich nitride.

15. (Currently Amended) A method of manufacturing a T-shaped gate conductor for an integrated circuit, the method comprising:

providing a first layer above a gate dielectric layer, the gate dielectric layer being above a substrate, the first layer including silicon and nitrogen;

providing a second layer above the first layer;

selectively etching ~~forming~~ a first aperture in the second layer by etching;

selectively etching ~~forming~~ a second aperture in the first layer utilizing an etching process the second aperture being narrower than the first aperture;

filling the first aperture and the second aperture with a gate conductor material; and

removing the gate conductor material above the second layer, thereby leaving the T-shaped gate conductor in the first and second aperture.

16. (Previously Amended) The method of claim 15, wherein:

the second layer is an oxide layer.

17. (Original) The method of claim 16, wherein the gate conductor material is doped or undoped polysilicon material.

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18. (Previously Amended) The method of claim 17, wherein etching the second aperture uses a RELACS process.

19. (Previously Amended) The method of claim 16, wherein the gate conductor material is silicided.

20. (Original) The method of claim 16, wherein the oxide layer is silicon dioxide.

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